Amendments to the Claims

Please cancel claims 1-6 and 17-21. The currently pending claims after amendment are listed below.

1 - 6. (Cancelled)

7. (Previously Presented) A method of eliminating parasitic bipolar transistor action in a Silicon on Insulator (SOI) Metal Oxide Semiconductor (MOS) dynamic logic circuit having an input, an output, a clock, an active discharge transistor, and a plurality of stacked SOI Metal Oxide Semiconductor (MOS) transistors interconnected to define a common node and an intermediate node, wherein:

said plurality of stacked SOI MOS transistors is controlled by a plurality of inputs;

said common node is coupled to a pre-charging device;

said intermediate node is in a path between said common node and a voltage source, said path defined by said plurality of stacked SOI MOS transistors;

said intermediate node is coupled to said common node by at least a first of said plurality of stacked SOI MOS transistors; and

said active discharging transistor is controlled by at least one of said plurality of inputs, said active discharging transistor defining a discharge path between said intermediate node and said voltage source,

the method comprising:

controlling the conduction of said active discharging transistor during a pre-charge cycle; and

actively discharging said intermediate node, whereby the parasitic bipolar transistors are deactivated and the charge at said intermediate node is maintained at a predetermined level.

8. (Original) The method according to claim 7, wherein pre-charging occurs during a low state of said clock.

9. (Original) The method according to claim 7, wherein pre-charging occurs during a high state of said clock.

10. (Original) The method according to claim 7, wherein during the pre-charging all said inputs are set to a predetermined logic state.

11. (Original) The method according to claim 10, wherein said logic state is low.

12. (Original) The method according to claim 10, wherein said logic state is high.

13. (Original) The method according to claim 7, wherein the step of actively discharging said intermediate nodes prevents the body voltages of said stacked SOI transistors from reaching a voltage stage sufficient to activate the parasitic bipolar transistors of said stacked SOI transistors.

14. (Original) The method according to claim 7, wherein said stacked transistors are N-Field Effect Transistors (NFET) and said active discharging transistors are P-Field Effect Transistors (PFET).

15. (Original) The method according to claim 7, wherein said stacked transistors are P-Field Effect Transistors (PFET) and said active precharging transistors are N-Field Effect Transistors (NFET).

16. (Original) The method according to claim 7, wherein said pre-charging device comprises transistors coupled to said stacked transistors.

17 - 21. (Cancelled)